



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,636	10/10/2003	Nadeem N. Eleyan	004-30059	1191

22120 7590 08/01/2005

ZAGORIN O'BRIEN GRAHAM LLP
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER

LE, THONG QUOC

ART UNIT	PAPER NUMBER
----------	--------------

2827

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center">Office Action Summary</p>	Application No. 10/683,636	Applicant(s) ELEYAN ET AL.	
	Examiner Thong Q. Le	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 and 24-42 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-22, 24 and 25 is/are allowed.
- 6) ☒ Claim(s) 1-7 and 26-42 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/8/05</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

1. Amendment filed on 06/08/2005 has been entered.
2. Claims 1-22, 24-42 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-22, 23-42 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

4. This office acknowledges receipt of the following items from the Applicant:
Information Disclosure Statement (IDS) filed on 6/08/2005.
5. Information disclosed and list on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-7,26-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Sadayuki (U.S. Patent No. 6,519,175).

Regarding claims 1, 26, 41-42, Sadayuki discloses a test block (Figure 10) for a memory circuit, wherein the test block is configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistor (Figure 1, 20A, Column 56-67, Column 4, lines 1-21, Column 15, lines 30-58).

Regarding claims 2-7, 27-40, Sadayuki discloses wherein the test block selectively introduces discharge paths into respective halves of differential circuit sensed by the sensing circuit (Column 11, lines 40-63), and wherein the discharge paths are selectively introduced to characterize a direction of the sensing offset or a magnitude of the sensing offset (Column 7, lines 1-65, Column 5, lines 60-67, Column 6, lines 1-24), and wherein the sensing offset results, at least in part, from accumulated data-dependent mismatch in characterize of the cross-coupled transistors(column 12, lines 1-18), and wherein the sensing offset results, at least in part, from a disparate, negative bias temperature instability induced shift in threshold voltage (V_t) of at least one of the cross-coupled transistors based on disparate voltage bias histories thereof (Figures 7-8 Column 12, lines 1-65), and wherein the sensing offset results, at least in part, from process variations in either the transistors or differential pair circuits to which the transistors are coupled (Column 11, lines 25-58).

Allowable Subject Matter

8. Claims 8-22, 24-25 are allowed.

Claims 8-22,24-25 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Sadayuki (U.S. Patent No. 6,519,175), and others, does not teach the claimed invention having at least a first and a second discharge path coupled to at least one of the respective first and second plurality of ports, and the effective strengths of the first and second discharge paths determined by respective ones of the first and second plurality of control signals, the first and second discharge paths configurable for characterization of a sensing offset associated with a sensing circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827

**THONG LEI
PRIMARY EXAMINER**